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**In the Specification:**

Please amend the paragraph beginning on page 9, line 26 as follows:

An alternate exemplary process flow for fabricating the Peltier devices 14, 16 and 18 in accordance with the present invention may be understood by referring now to FIGS. 13-18 and initially to FIG. 13. Again, the description will be in the context of the Peltier device 18, but will be illustrative of the other devices 14 and 16 as well. Turning now to FIG. 13, fabrication of the interconnect layer 38 may be substantially as described above. Thereafter, an insulating film 82 is formed over the interconnect layer 38. A variety of well-known insulator materials may be used such as, for example, TEOS, silane-based oxide, doped glasses or the like. In an exemplary embodiment, TEOS is deposited by CVD to a depth of about 6,000 to 14,000 Å and within that thickness range such that the film 34 completely covers the impurity regions 46, 48, 50 and 52 as shown. A suitable etch mask 84 composed of photoresist is next patterned on the insulator film 82 with openings ~~84~~ 85 and 86 corresponding to the desired layouts for the impurity regions 50 and 52 as represented by the dashed boxes 88 and 90.